Electron Beam Mask Writer EBM-9500PLUS for logic 7nm+ node generation

Hideki Matsui*, Kota Iwasaki, Noriaki Nakayamada, Takashi Kamikubo, Keita Ideno, Michihiro Kawaguchi, Kiyoshi Nakaso, Takahito Nakayama, Takanao Touya, Taku Yamada, Toru Hinata and Kenji Ohtoshi.

NuFlare Technology, Inc., 8-1 Shinsugita, Isogo, Yokohama, Kanagawa 235-8522, Japan

NuFlare's EB mask writer roadmap

> Full production lineup is ready for sales.



Charging Effect Reduction (CER)

- > CER technology was developed for EBM-9500PLUS.

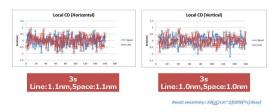
 - H/W modification : To reduce fogging charging
 New CEC model : To compensate re-entering low-energy secondary electron charging

CER achieves image placement performance equivalent to CDL results.



Local CD accuracy

- Evaluation by 120nm width space in local area on mask.
- Line: measurement between exposed lines.
- Space: measurement on exposed line.
- Achieved EBM-9500PLUS standard specification, (1.3[nm])



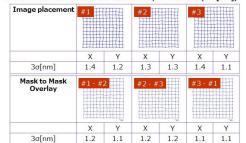
Motivation for development

- > Target technology Node: 7 nm+
- > Key development: Improvement of Image Placement error

| | EBM-8000P/M | EBM-8000P/H | EBM-9000 | EBM-9500 | EBM- 9500PLUS |
|--|---------------|--------------|--------------|---------------|------------------|
| Technology node | 45-20nm | 14/16nm | 10nm | 7nm | 7nm+ |
| Current density [A/cm ²] (Total current[nA]) | 400 (1000) | 400 (490) | 800 (500) | 1200 (750) | 1200 (750) |
| Max shot size [nm] | 500 | 350 | 250 | 250 | 250 |
| LCD* [3 ₀] | 2.5nm | 1.3nm | 1.3nm | 1.3nm | 1.3nm |
| IP [3 ₀] | 6nm | 4.3nm | 3.0nm | 2.1nm | 1.8nm** |
| Writing time[H]*** | 12.0 | 12.0 | 6.5 | 6.0 | 6.0 |

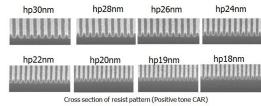
Global image placement with low-density layout

> Achieved EBM-9500PLUS standard specification. (1.8[nm])



Patterning resolution

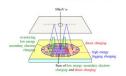
> Less than 30[nm] were resolved.

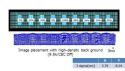


Problem statement for Image Placement error

- Resist charging is dominant error source for image placement error.
- NuFlare's mask writer use Charging Effect Correction (CEC) S/W to compensate resist charging error.
 - Correction residual error is error source for position accuracy.
 (Especially for complex patterns)
- Components of resist surface charging
 - > Direct charging

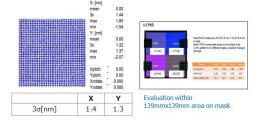
 - Fogging charging
 Re-entering low-energy secondary electron charging





Global position with high-density layout

- > 4 different density pads are placed in global.
- Achieved EBM-9500PLUS standard specification (1.8[nm])



Conclusion

- > We developed EBM-9500PLUS for 7nm+ tn generation.
 - > Charging Effect Reduction (CER) technology is newly introduced to improve Image Placement error with high-density layouts.
 - > CER achieves image placement performance equivalent to CDL performance.
- Nuflare confirmed performance of EBM-9500PLUS.
- > EBM-9500PLUS meets standard specification.
 - > Local CD : 1.3[nm]
 - > Global IP with high-density layouts: 1.8[nm]
- > Released for sale on Oct, 2018.

NuFlare Technology,Inc.